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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,205	01/26/2004	Nobuaki Hashimoto	118212	6430

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,205	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al. (US 6,835,595 B1).

3. Regarding Claim 1, Suzuki et al. disclose a semiconductor device comprising:

a semiconductor substrate (1) (Figure 3) that includes an active element region, an integrated circuit having an active element in the active element region (Col. 4, lines 28, lines 28 – 35) and an electrode (2) electrically connected to the integrated circuit,

a resin layer (3,4) that is formed on a surface of the semiconductor substrate where the electrode (2) is also formed, so as to avoid the electrode,

a wiring layer (6) that extends from the electrode and across a top of the resin layer (4) and includes a plurality of electrically connecting portions, the plurality of electrically connecting portions including a first electrically connecting portion (under bump 11) and a second electrically connecting portion (over 2), a surface area of the first electrically connecting portion being larger than a surface area of the second electrically connecting portion, and

an external terminal (11) that is provided on the electrically connecting portion.

4. Regarding Claim 2, Suzuki et al. disclose that the second electrically connecting portion is formed on a top surface of the resin layer (3).

5. Regarding Claim 3, Suzuki et al. disclose the resin layer (4) overlapping the active element region of the semiconductor substrate and the first electrically connecting portion (under bump 11) formed on the area of the resin layer that overlaps the active element region.

6. Regarding Claim 4, Suzuki et al. disclose that the first electrically connecting region is formed so as to cover the entire top surface of the resin layer (4).

7. Regarding Claim 5, Suzuki et al. disclose that the first electrically connecting portion covers a side surface of the resin layer (4) (See Figure 3).

8. Regarding Claim 6, Suzuki et al. disclose that the first electrically connecting portion (under bump 11) is formed so as to extend the region beyond the resin layer (4).

9. Regarding Claim 7, Suzuki et al. do not explicitly disclose that the first electrically connecting portion supplies a power source potential. However for the plurality of sites available on the integrated circuit, it is implicit that at least one of the (contact pad) sites supplies power to the circuit so that a working device is present.

10. Regarding Claim 8, Suzuki et al. disclose that the first electrically connecting portion is formed in a shape and size (Col. 5, line 65 through Col. 6, line 15) to provide uniform conductivity and stress reduction.

11. Regarding Claim 9, Suzuki et al. disclose the presence of an insulating layer (8) formed to cover the wiring layer while avoiding the external terminal (11).

12. Regarding Claim 10, Suzuki et al. disclose that the semiconductor substrate is a semiconductor wafer (Col. 4, lines 28 – 32).

13. Regarding Claim 11, Suzuki et al. disclose a semiconductor device comprising:

a semiconductor substrate (1) (Figure 3) that includes an active element region, an integrated circuit having an active element in the active element region (Col. 4, lines 28, lines 28 – 35) and an electrode (6) electrically connected to the integrated circuit, where the electrode (2) is also formed, so as to avoid the electrode,

a resin layer (3,4) that is formed on a surface of the semiconductor substrate where the electrode (2) is also formed, so as to avoid the electrode,

a wiring layer (6) that extends from the electrode and across a top of the resin layer (4) and includes a plurality of electrically connecting portions, the wiring layer including a first electrically connecting portion (under bump 11) and a second electrically connecting portion (over 2), the first electrically connecting portion covering the entire surface of the resin layer except for the area occupied by the wiring layer including the second electrically connecting

portion (over 2) and the area surrounding the wiring layer including the electrically connecting portion, and

an external terminal (11) that is provided on the electrically connecting portion.

14. Regarding Claim 12, Suzuki et al. disclose that a circuit board is connected to the semiconductor device (Col. 3, lines 24 – 26).

15. Regarding Claim 13, Suzuki et al. disclose that the electronic device is a semiconductor device (integrated circuit) (Col. 4, lines 30 – 31).

16. Regarding Claim 14, Suzuki et al. disclose a method of manufacturing a semiconductor device comprising:

forming a resin layer (3,4) on a surface of the semiconductor substrate (1) (Figure 3) including an active element region, an integrated circuit having an active element in the active element region (Col. 4, lines 28, lines 28 – 35) and an electrode (6) electrically connected to the integrated circuit (at 2), the resin layer being formed, so as to avoid the electrode,

extending a wiring layer (6) from the electrode and across a top of the resin layer (4) making the wiring layer include a plurality of electrically connecting portions,

providing an external terminal (11) on the electrically connecting portion, and

forming the plurality of electrically connecting portions so that a surface area of the first electrically connecting portion is larger than a surface area of the second electrically connecting portion (See Figure 3).

Conclusions

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
April 12, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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